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10/813,628	03/31/2004	Simon Knowles	ICER-321538	3813

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EXAMINER	
FRANKLIN, RICHARD B	

ART UNIT	PAPER NUMBER
2181	

NOTIFICATION DATE	DELIVERY MODE
07/02/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/813,628	KNOWLES, SIMON	
	Examiner	Art Unit	
	RICHARD FRANKLIN	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/21/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 29 are pending.

Response to Arguments

2. Applicant's arguments with respect to claims 1 – 29 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

3. Claims 1, 2, and 26 are objected to because of the following informalities:

a. Claim 1 Lines 15 – 16: The claim reads "comprises at least two control ***instructions said*** control instructions" (emphasis added). It appears a comma [,] would be appropriate between “instructions” and "said” to aid in the reading clarity of the claim.

b. Claim 2 Lines 3 – 4: The claim reads “the decode unit is operable to ***supply for execution each of the three control instructions***" (emphasis added). The wording of the claim appears to be awkward. The Examiner suggests something such as “the decode unit is operable to ***supply each of the three control instructions for execution***” as an alternate wording choice.

c. Claim 26 Line 12: The claim reads “the instruction packet is of a ***first which*** defines:” (emphasis added). It appears Applicant has omitted the word "class" between "first" and "which" to define “a first class.”

d. Claim 26 Lines 16 – 17: The claim reads "the instruction packet comprises at least two control ***instructions supplying*** said at least two control instructions" (emphasis added). It appears a comma [,] would be appropriate between "instructions" and "supplying" to aid in the reading clarity of the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 – 3, 6 – 10, 12, 14, 16, 17, 19, and 21 – 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 7,234,042 (hereinafter Wilson) in view of US Patent No. 6,292,845 (hereinafter Fleck.)

As per claims 1 and 26 – 28, Wilson teaches a computer processor (Wilson; Figure 1), the processor comprising (a) a decode unit (Wilson; Figure 1 Item 4) for decoding a stream of instruction packets from a memory (Wilson; Figure 1 Item 2), each instruction packet comprising a plurality of instructions (Wilson; Col 3 Lines 48 – 50); (b) a first processing channel (Wilson; Figure 1 Items 6_x and 8_x) comprising a plurality of functional units (Wilson; Figure 1 Items 6_x and 8_x) and operable to perform control processing operations (Wilson; Col 4 Lines 7 – 10); (c) a second processing channel (Wilson; Figure 1 Items 6_y and 8_y) comprising a plurality of functional units (Wilson;

Figure 1 Items 6_y and 8_y) and operable to perform data processing operations (Wilson; Col 4 Lines 7 – 10) and; wherein the decode unit is operable to receive instruction packets sequentially (Wilson; Col 3 Lines 46 – 48) and to detect if each instruction packet is of a first class which defines (i) at least two control instructions (Wilson; Col 4 Lines 51 – 57 "two load/store operations (ID1, ID2 both set to '1')") or a second class which defines (ii) a plurality of instructions one or more of which is a data processing instruction (Wilson; Col 4 Lines 51 – 57 "two data processing operations (ID1, ID2 both set to '0')"), the decode unit using at least one identification bit at a predetermined bit location in the packet for detecting if the instruction packet is of the first or second class (Wilson; Col 4 Lines 48 – 51), and wherein when the decode unit detects that the instruction packet is of the second class, said plurality of instructions are executed simultaneously (Wilson; Col 6 Lines 31 – 41).

Wilson does not teach wherein when the decode unit detects that the instruction packet comprises at least two control instructions said control instructions are supplied to the first processing channel for execution in program order.

However, Fleck teaches wherein when two control instructions are follow one another, the decode unit issues them to a first processing channel in program order (Fleck; Col 3 Lines 47 – 60, Col 6 Lines 27 – 28).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Wilson to include processing the control instructions in program order because doing is easily implemented (Fleck; Col 3 Lines 59 – 61).

As per claim 2, Fleck also teaches wherein when the decode unit detects that the instruction packet comprises three control instructions, the decode unit is operable to supply for execution each of the three control instructions in the order in which they appear in the instruction packet (Fleck; Col 3 Lines 34 – 52; Examiners note: Since the instruction buffer contains four instructions and the instructions may be of the same type, it is clear that Fleck discloses the ability to decode three control instructions).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Wilson to include processing the control instructions in program order because doing is easily implemented (Fleck; Col 3 Lines 59 – 61).

As per claim 3, Wilson also teaches wherein the decode unit is operable to detect that the instruction packet contains a plurality of control instructions of equal length (Wilson; Col 4 Lines 45 – 48).

As per claim 6, Wilson also teaches wherein the decide unit is operable to receive and decide instruction packets of a bit length of 64 bits (Wilson; Col 3 Lines 48 – 50).

As per claim 7, Wilson also teaches wherein the decode unit is operable to detect when there is at least one data processing instruction in the instruction packet (Wilson;

Col 4 Lines 48 – 57) and, in response thereto, to cause relevant data to be supplied to the second processing channel (Wilson; Col 6 Lines 38 – 41).

As per claim 8, Wilson also teaches wherein the decide unit is operable to detect that the instruction packet of the second class comprises at least one processing instruction and a further instruction selected from one or more of: a memory access instruction; a command instruction (Wilson; Col 4 Lines 51 – 57 “one data processing and one load/store operation(ID1=0, ID2=1)”); and a further data processing instruction (Wilson; Col 4 Lines 51 – 57 “two data processing operations (ID1, ID2 both set to ‘0’)”).

As per claim 9, Wilson also teaches wherein at least one data processing instruction and said further instruction are executed simultaneously (Wilson; Col 6 Lines 31 – 41).

As per claims 10 and 25, Fleck teaches the second processing channel performs data processing operations (Fleck; Col 3 Lines 30 – 32) and data processing instructions are provided in assembly language (Fleck; Col 4 Lines 63 – 67; Examiner's Note: It would have been common at the time of invention to require the instructions to be written in assembly code as was a common standard at the time of invention.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Wilson to include the assembly instructions because doing is easily implemented (Fleck; Col 3 Lines 59 – 61).

As per claim 12, Wilson also teaches wherein the first processing channel comprises units selected from one or more of: a control register file; a control execution unit; a branch execution unit; and a load/store unit (Wilson; Figure 1 Item 6_x).

As per claim 14, Fleck also teaches wherein the second processing channel comprises a data execution path including a fixed data execution unit (Fleck; Figure 1 Item 11).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Wilson to include fixed data execution unit because doing is easily implemented (Fleck; Col 3 Lines 59 – 61).

As per claim 16, Wilson also teaches wherein the data execution unit operates according to single instruction multiple data principles (Wilson; Col 3 Lines 55 – 60).

As per claim 17, Wilson also teaches wherein the second processing channel comprises one or more of a data register file and a load/store unit (Wilson; Figure 1 Item 6_y).

As per claim 19, Wilson also teaches wherein the decode unit is operable to detect that the instruction packet of the second class comprises at least one data processing instruction having a bit length between 30 and 38 bits (Wilson; Col 45 – 48).

As per claim 21, Fleck also teaches wherein the decode unit is operable to detect that the instruction packet comprises a data processing instruction (Fleck; Col 4 Lines 11 – 16) and a memory access instruction (Fleck; Col 4 Lines 11 – 16).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Wilson to include the data processing and memory access instructions because doing is easily implemented (Fleck; Col 3 Lines 59 – 61).

As per claim 22, Wilson in combination with Fleck teaches the computer processor as described per claim 21 (see rejection of claim 21 above).

Fleck Wilson in combination with Fleck does not explicitly disclose the bit length of said memory access instruction is 28 bits.

However, it would have been obvious to one of ordinary skill in the art at the time of invention that the bit lengths of instructions disclosed in Wilson in combination with Fleck are of little significance and the primary concern set forth by Wilson in combination with Fleck is merely the separation of instructions within the packet.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a smaller instruction size than 32 bits in the invention disclosed by Wilson and Fleck with the goals of either saving space or adapting the invention to a customized standard. Furthermore, it would have been obvious to one of ordinary skill in the art at the time of invention that the size of an individual word is of no

consequence given the words are still separated properly as disclosed by Wilson and Fleck.

As per claim 23, Wilson also teaches wherein the decode unit is operable to detect that the instruction packet of the second class comprises at least one data processing instruction and at least one a-control instruction (Wilson; Col 4 Lines 51 – 57 “one data processing and one load/store operation(ID1=0, ID2=1)”).

As per claim 24, Wilson in combination with Fleck teaches the computer processor as described per claim 1 (see rejection of claim 1 above).

Wilson in combination with Fleck does not explicitly disclose the decode unit being operable to detect a control processing instruction in C code or variant thereof.

However, it would have been obvious to one of ordinary skill in the art at the time of invention to enable a processor to support higher level languages, such as C, as the languages are easier to develop code in and are more commonly used to develop code in. Therefore, it would have been obvious to allow a user to utilize an easier language such as C to code control instructions.

As per claim 29, Wilson teaches a computer including a first class of instruction packets each comprising two or more control instructions (Wilson; Col 4 Lines 51 – 57 “two load/store operations (ID1, ID2 both set to ‘1’)”) and a second class of instruction packets each comprising at least a data processing instruction and a further instruction

(Wilson; Col 4 Lines 51 – 57 "two data processing operations (ID1, ID2 both set to '0')") for execution contemporaneously (Wilson; Col 6 Lines 31 – 41), wherein instruction packets contain at least one identification bit at a predetermined bit location in the packet for detecting if the instruction packet is of the first or second class (Wilson; Col 4 Lines 48 – 51).

Wilson does not teach wherein the first class of instruction packet is executed sequentially.

However, Fleck teaches wherein when two control instructions are follow one another, the decode unit issues them to a first processing channel in program order (Fleck; Col 3 Lines 47 – 60, Col 6 Lines 27 – 28).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Wilson to include processing the control instructions in program order because doing is easily implemented (Fleck; Col 3 Lines 59 – 61).

5. Claims 4 – 5 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 7,234,042 (hereinafter Wilson) in view of US Patent No. 6,292,845 (hereinafter Fleck) and further in view of US Patent No. 6,880,150 (hereinafter Takayama).

As per claim 4, Wilson in combination with Fleck teaches the computer processor as described per claim 3 (see rejection of claim 3 above).

Wilson in combination with Fleck does not teach detecting within an instruction packet a control instruction of a bit length between 18 and 24 bits.

However, Takayama teaches detecting within an instruction packet a control instruction of a bit length between 18 and 24 bits (Takayama; Col 13 Lines 29 – 33).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Wilson in combination with Fleck to include the control packet of between 18 and 24 bits in length because doing so allows for control instructions to be executed even when other operations are performed in units of an integer number of bytes (Takayama; Col 2 Lines 9 – 13) which increases execution speed of control instructions and thus the entire system.

As per claim 5, Takayama also teaches detecting within an instruction packet a plurality of control instructions each having a bit length of 21 bits (Takayama; Col 13 Lines 29 – 33).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Wilson in combination with Fleck to include the control instructions having 21 bits in length because doing so allows for control instructions to be executed even when other operations are performed in units of an integer number of bytes (Takayama; Col 2 Lines 9 – 13) which increases execution speed of control instructions and thus the entire system.

As per claim 11, Wilson in combination with Fleck teaches the computer processor as described per claim 1 (see rejection of claim 1 above).

Wilson in combination with Fleck does not teach control processing operations being performed on operands up to a first predetermined bit width and the data processing operations being performed on data up to a second pre-determined bit width, the second pre- determined bit width being larger than the first pre-determined bit width.

However, Takayama teaches control processing operations being performed on operands, up to a first predetermined bit width and the data processing operations being performed on data up to a second pre-determined bit width, the second pre-determined bit width being larger than the first pre-determined bit width (Takayama; Col 13 Lines 29 – 33; Examiner's note: Use of 21-bit and 42-bit instructions.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Wilson in combination with Fleck to include the pre-determined bit widths because doing so allows for control instructions to be executed even when other operations are performed in units of an integer number of bytes (Takayama; Col 2 Lines 9 - 13).

6. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 7,234,042 (hereinafter Wilson) in view of US Patent No. 6,292,845 (hereinafter Fleck) and further in view of US Patent No. 6,725,357 (hereinafter Cousin).

As per claim 18, Wilson in combination with Fleck teaches the computer processor as described per claim 1 (see rejection of claim 1 above).

Wilson in combination with Fleck does not teach wherein a single load/store unit is accessed by both channels through respective ports.

However, Cousin teaches two processing channels which access a single common load/store unit through respective ports (Cousin; Figure 3 Item 150).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Wilson in combination with Fleck to include the single load/store unit because doing so allows for the channels to work together to accomplish instructions (Cousin; Col 5 Line 56 – Col 6 Line 4).

7. Claims 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patent No. 7,234,042 (hereinafter Wilson) in view of US Patent No. 6,292,845 (hereinafter Fleck) and further in view of US Patent No. 5,956,518 (hereinafter DeHon).

As per claim 13, Wilson in combination with Fleck teaches the computer processor as described per claim 1 (see rejection of claim 1 above).

Wilson in combination with Fleck does not teach the second processing channel comprising a data execution path including a configurable data execution unit.

However, DeHon teaches a data execution path including a configurable data execution unit (DeHon; Col 5 Lines 23 – 26).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Wilson in combination

with Fleck to include the configurable data execution unit because doing so allows for greater flexibility for processing ability (DeHon; Col 1 Lines 41 – 47).

As per claim 15, DeHon also teaches wherein the configurable data execution unit operates according to single instruction multiple data principles (DeHon; Col 5 Lines 23 – 26).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Wilson in combination with Fleck to include the SIMD principles because doing so allows for greater flexibility for processing ability (DeHon; Col 1 Lines 41 – 47).

8. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 7,234,042 (hereinafter Wilson) in view of US Patent No. 6,292,845 (hereinafter Fleck) and further in view of "Variable Length Instruction Compression for Area Minimization", Piia Simonen, Ilkka Saastamoinen, Jari Nurmi, 2003, IEEE (hereinafter Simonen).

As per claim 20, Wilson in combination with Fleck teaches the computer processor as described per claim 19 (see rejection of claim 19 above). Wilson in combination with Fleck further disclose the decode unit being operable to detect an instruction packet comprising at least one data processing instruction (Wilson; Col 4 Lines 48 – 57).

Wilson in combination with Fleck does not teach a bit length of the at least one data processing instruction is 34 bits.

However, Simonen teaches a bit length of the at least one data processing instruction is 34 bits (Simonen; Section 3.1 ("Control Bits") Lines 3 – 4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Wilson in combination with Fleck to include the 34 bit data processing instruction because doing so allows for a reduction in the amount of space needed to implement certain data processing instructions (Simonen; Section 1 Lines 1 – 4, Section 3.1 Lines 5 – 7) which would increase overall processor throughput.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RICHARD FRANKLIN whose telephone number is (571)272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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